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**Jawaban**

1. .

library ieee;

use ieee.std\_logic\_1164.all;

entity adder\_3 is

    port(

        -- Input

        a : IN STD\_LOGIC; --MSB

        b : IN STD\_LOGIC;

        c : IN STD\_LOGIC;

        d : IN STD\_LOGIC; --LSB

        --output

        out\_a : OUT STD\_LOGIC;

        out\_b : OUT STD\_LOGIC;

        out\_c : OUT STD\_LOGIC;

        out\_d : OUT STD\_LOGIC

    );

end entity;

architecture adder\_3\_archi of *adder\_3* is

begin

    out\_a <= a OR (b AND c) OR (b AND d);

    out\_b <= (NOT b AND c) OR (NOT b AND d) OR (b AND NOT c AND NOT d);

    out\_c <= (b AND NOT d) OR (c AND d) OR (NOT a AND NOT c AND NOT d);

    out\_d <= (c AND NOT d) OR (NOT c AND NOT d);

end architecture;

1. .
2. 0101

A screenshot of a computer

Description automatically generated

1. 1100

A screenshot of a computer

Description automatically generated

1. 0011

A screenshot of a computer

Description automatically generated

1. 1010

A screenshot of a computer

Description automatically generated

1. .

A diagram of a computer program

Description automatically generated

A diagram of a machine

Description automatically generated

Keduanya sama intinya, tetapi pada sintesis RTL tidak menggunakan NOT, tetapi langsung NOT-nya di AND gatenya.

1. .

library ieee;

use ieee.std\_logic\_1164.all;

use  IEEE.STD\_LOGIC\_ARITH.ALL;

entity CS\_unsigned is

    port(

        -- Input

        input : IN STD\_LOGIC\_VECTOR (3 DOWNTO 0); --ini 4 bit, karena bit pertama dipake utk sign

        --output

        output : OUT STD\_LOGIC\_VECTOR (3 DOWNTO 0) --sama kayak input

    );

end entity;

architecture adder\_3\_archi of *CS\_unsigned* is

    signal in\_num : SIGNED (3 DOWNTO 0);

    signal out\_num: SIGNED (3 DOWNTO 0);

begin

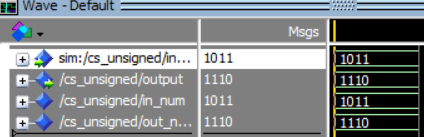
    in\_num <= signed(input);

    out\_num <= in\_num + 3;

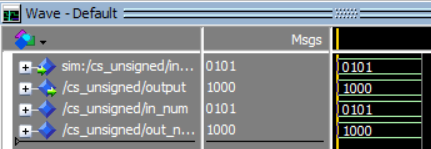
    output <= std\_logic\_vector(out\_num);

end architecture;

1. .
2. -5 (1 1011)

 Hasil 1110 (-2)

1. 5 ( 0101)

 Hasil 1000 (8)

1. -2 (1110)

A screenshot of a computer

Description automatically generated Hasil 0001 (1)

1. 3 (0011)

A screenshot of a computer

Description automatically generated Hasil 0110 (6)

1. .

* VHDL digunakan untuk buat rangkaian dengan kode
* STD\_LOGIC digunakan untuk menyimpan 1 bit data
* STD\_LOGIC\_VECTOR digunakan untuk menyimpan banyak bit data
* SIGN dan UNSIGN digunakan utk aritmatika, STD\_LOGIC\_VECTOR gak bisa aritmatika
* MODELSIM digunakan utk simulasi kode
* QUARTUS digunakan untuk melihat rangkaian yg dibuat